Listing of the Claims:

The following is a complete listing of all the claims in the application, with an indication of the status of each:

1 (Original). A simulation method for simulating a system having a plurality of circuit modules using software, comprising the steps of:

using an object oriented language;

preparing a plurality of circuit base classes, which describe base circuit modules as classes, as a library;

describing the circuit modules to be simulated as classes by inheriting the circuit base classes prepared as the library; and

describing the system to be simulated by combining the circuit modules described as the classes.

2 (Original). A simulation method according to claim 1, further comprising the step of describing the system as a class by inheriting the circuit base classes prepared in the library.

3 (Currently Amended). A simulation method according to claim 1, further comprising the step of preparing a component class having the properties of a circuit which contains a circuit operating asynchronously with a clock signal, and a synchronous module class, having the properties of a circuit operating synchronously with the clock signal in the library, which is derived from said component class.

4 (Original). A simulation method according to claim 3, further comprising the step of preparing a bus class having the properties of a bus, a bus master class having the properties of a bus master, and a bus slave class having the properties of a bus slave, as the circuit base class described as a class derived from the synchronous module class, in the library.

5 (Original). A simulation method according to claim 4, further comprising the step of preparing a bus master interface class, whose base classes are the synchronous module class, and which has the properties of a bus master interface, and a bus slave interface class having the properties of a bus slave interface, as the circuit base class in the library.

6 (Original). A simulation method according to claim 3, further comprising the step of preparing a central processing unit class, whose base class is the synchronous module class, and which has the properties of a central processing unit, as the circuit base class in the library.

7 (Original). A simulation method according to claim 3, further comprising the step of preparing a hierarchy class, whose base class is the synchronous module class, and which has the properties of a hierarchy of a circuit containing the bus, as the circuit base class in the library.

8 (Original). A simulation method according to claim 4, further comprising the step of preparing a memory class, whose base class is the bus slave class, and which has the properties of a memory, as the circuit base class in the library.

9. (Previously Presented). A simulating apparatus, using a computer, for simulating a system having a plurality of circuit modules, said simulation apparatus comprising:

storage means storing a plurality of circuit base classes, which describe base circuit modules as classes, as a library;

means accessing the storage means and describing the circuit modules to be simulated as classes by inheriting the circuit base classes stored in the library; and

means combining the circuit modules described as classes to describe the system to be simulated.

10 (Previously Presented). A computer-readable storage medium for storing a computer program for executing a simulation method for simulating a system having a plurality of circuit modules, the computer program comprising the steps of:

using an object oriented language;

preparing a plurality of circuit base classes, which describe base circuit modules as classes, as a library;

describing the circuit modules to be simulated as classes by inheriting the circuit base classes prepared as a library; and

describing the system to be simulated by combining the circuit modules described as classes.

11 (New). A simulating apparatus according to claim 9, wherein the means combining the circuit modules describes the system to be simulated as a class by inheriting the circuit base classes prepared in the library.

12 (New). A simulating apparatus according to claim 9, wherein the storage means stores a component class having the properties of a circuit which contains a circuit operating asynchronously with a clock signal, and a synchronous module class, having the properties of a circuit operating synchronously with the clock signal in the library, which is derived from said component class.

13 (New). A simulating apparatus according to claim 12, wherein the storage means stores a bus class having the properties of a bus, a bus master class having the properties of a bus master, and a bus slave class having the properties of a bus slave, as the circuit base class described as a

class derived from the synchronous module class, in the library.

14 (New). A simulating apparatus according to claim 13, where in the storage means stores a bus master interface class, whose base classes are the synchronous module class, and which has the properties of a bus master interface, and a bus slave interface class having the properties of a bus slave interface, as the circuit base class in the library.

15 (New). A simulating apparatus according to claim 12, wherein the storage means stores a central processing unit class, whose base class is the synchronous module class, and which has the properties of a central processing unit, as the circuit base class in the library.

16 (New). A simulating apparatus according to claim 12, wherein the storage means stores a hierarchy class, whose base class is the synchronous module class, and which has the properties of a hierarchy of a circuit containing the bus, as the circuit base class in the library.

17 (New). A simulating apparatus according to claim 13, wherein the storage means stores a memory class, whose base class is the bus slave class, and which has the properties of a memory, as the circuit base class in the library.

18 (New). A computer-readable storage medium according to claim 10, wherein the computer program further comprises the step of describing the system as a class by inheriting the circuit base classes prepared in the library.

19 (New). A computer-readable storage medium according to claim 10, wherein the computer program further comprises the step of preparing a

component class having the properties of a circuit which contains a circuit operating asynchronously with a clock signal, and a synchronous module class, having the properties of a circuit operating synchronously with the clock signal in the library, which is derived from said component class.

20 (New). A computer-readable storage medium according to claim 19, wherein the computer program further comprises the step of preparing a bus class having the properties of a bus, a bus master class having the properties of a bus master, and a bus slave class having the properties of a bus slave, as the circuit base class described as a class derived from the synchronous module class, in the library.

21 (New). A computer-readable storage medium according to claim 20, wherein the computer program further comprises the step of preparing a bus master interface class, whose base classes are the synchronous module class, and which has the properties of a bus master interface, and a bus slave interface class having the properties of a bus slave interface, as the circuit base class in the library.

22 (New). A computer-readable storage medium according to claim 19, wherein the computer program further comprises the step of preparing a central processing unit class, whose base class is the synchronous module class, and which has the properties of a central processing unit, as the circuit base class in the library.

23 (New). A computer-readable storage medium according to claim 19, wherein the computer program further comprises the step of preparing a hierarchy class, whose base class is the synchronous module class, and which has the properties of a hierarchy of a circuit containing the bus, as the circuit base class in the library.

24 (New). A computer-readable storage medium according to claim 20, wherein the computer program further comprises the step of preparing a memory class, whose base class is the bus slave class, and which has the properties of a memory, as the circuit base class in the library.